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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,948	02/06/2004	S. Babar Raza	CYPR-CD02209	2169
7590 01/14/2008 WAGNER, MURABITO & HAO LLP Third Floor Two North Market Street San Jose, CA 95113			EXAMINER NGUYEN, HANH N	
			ART UNIT 2616	PAPER NUMBER
			MAIL DATE 01/14/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/773,948

Applicant(s)

RAZA, S. BABAR

Examiner

Hanh Nguyen

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on Amendment filed on 11/5/07.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19 and 20 is/are allowed.
- 6) ☒ Claim(s) 1, 3, 12, 15, 16 is/are rejected.
- 7) ☒ Claim(s) 2, 4-11, 13, 14, 17 and 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 November 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claim 1, it appears that "port frequency" is not disclosed in the specification. However, the specification on page 12, lines 15-20, discloses "port clock". According to the specification on page 12, lines 15-20, it is noted that data at port clock associated with port synchronization logic devices is synchronized to core clock at single memory core. Therefore, applicant needs to indicate that the information is synchronized between port clocks associated with synchronization logic device and core clock associated with the single port memory core.

Claims 2-11 are rejected because they depend on claim 1 respectively.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3, 12, 15, 16 are rejected under 35 USC 103(a) as being unpatentable over Raza et al. ( US pat. 7,016,349 B1) in view of De Korte et al. ( US pat. 5,822,776).

In claims 1 and 12, Raza et al. discloses a memory device ( system 100; fig.2) comprising: a first and a second port synchronization logic devices associated with a first and second port, respectively ( see fig.2, col.5; lines 18-25; write interface 104 having port data-in and read interface 106 having port data-out are implemented as data synchronize logic devices); and a single-ported memory ( see fig.2; col.5, lines 1-7; memory 102 is implemented as single port memory). Raza et al. disclose the first and second port synchronization logic devices synchronize information communicated between the first and second port associated with the first and second port synchronization logic devices and the single-ported memory core by synchronizing information between port clocks and core clocks that is associated with the single port memory core (It is noted that this limitation is examined based on disclosure in specification, page 12, lines 15-30. See fig.2, the write interface 104 and read interface 106 are separate clock domains representing WR\_CLK\_DOMAIN and RD\_CLK\_DOMAIN ( see col.5, lines 30-40), wherein synchronization is performed by the two clock domains by writing data from write interface 104 into the single port memory 102 and reading data out from read interface 106 via memory 102. The data synchronization is controlled by logic domain 108( col.7, lines 45-60)). Raza et al. also

discloses a dual port memory core 100" ( see fig.6). Raza et al. does not disclose the single port memory core 102 is coupled a port multiplexing logic.

De Korte et al. discloses a single port RAM 1 ( see fig.1) is implemented as RAM 1 shown in fig.3 with dataport 8 coupled to a mux 20 via address/control signals( a single port memory is coupled to port multiplexer logic). Therefore, it would have been obvious to couple the mux 20 of De Korte et al. with the single port memory 102 of Raza et al. so that data synchronization between synchronization logic devices and the single port memory core is performed.

In claim 3, with the combination of Raza et al., De Korte et al. discloses a bus for communicating between port multiplexer logic and the single port memory core ( see fig.3).

In claims 15 and 16, Raza et al. discloses the first port synchronization logic device comprises a read data and control FIFO circuit ( see fig.1; read interface) ; a write data and control FIFO circuit ( write interface) ; and an address FIFO circuit ( FIFO 16).

### ***Allowable Subject Matter***

Claims 2, 4-11, 13, 14, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Response to Arguments***

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Applicant's arguments with respect to claims 1-18 have been considered but claims 1, 3, 12, 15, 16 are moot in view of the new ground(s) of rejection.

***Allowable Subject Matter***

Claims 19, 20 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dougherty et al. ( Us pat. 7,242,686 B1);

Payson ( US pat. 7,193,994 B1).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh Nguyen whose telephone number is 571 272 3092. The examiner can normally be reached on Monday-Thursday from 8:30 to 4:30PM. The examiner can also be reached on alternate

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild, can be reached on 5712723092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hanh Nguyen

A handwritten signature in black ink, appearing to read 'H. Nguyen', with a stylized flourish at the end.

**HANH NGUYEN**  
**PRIMARY EXAMINER**